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AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A component, containing comprising:

[[[-]]] a chip (CH) having a top surface and having a bottom surface that includes electrically conductive structures; ~~on the underside of the chip~~,

[[[-]]] a carrier substrate (TS), which has having a top surface that includes connecting areas (AF) ~~on the surface~~, with the chip (CH) being mounted in a flip chip arrangement on the carrier substrate via ~~by means~~ of electrically conductive connections between (BU), ~~and with the connecting areas (AF) being electrically connected to the~~ electrically connective conductive structures and the connecting areas; of the chip by means of electrically conductive connections (BU),

[[[-]]] a support element on the top surface of the carrier substrate, the support element surrounding, (SE) to relieve the electrically conductive connections, which is positioned on the top side of the carrier substrate and encircles the chip without but not touching, the carrier substrate; and it,

[[[-]]] a seal (AB) which that surrounds the chip and tightly closes at least the space between the support element; and the aforementioned chip, with wherein the seal being supported on this support element supports the seal.

2. (Currently Amended) The component ~~as recited in of~~ claim 1, wherein the electrically conductive connections ~~are~~ comprise bumps.

3. (Currently Amended) The component ~~as recited in of~~ claim 1 ~~or 2~~, wherein the seal (AB) ~~is designed as~~ comprises a dielectric layer ~~which also~~ and substantially covers the top ~~side~~ surface of the chip.

4. (Currently Amended) The component ~~as recited in of~~ claim 3, wherein the dielectric layer ~~consists of~~ comprises one or more layers.

5. (Currently Amended) A component, ~~containing~~ comprising:
[[-]] a chip (CH) ~~having a top surface and having a bottom surface that includes~~ electrically conductive structures; ~~on the underside of the chip,~~
[[-]] a carrier substrate (TS), ~~which has~~ having a top surface that includes connecting areas (AF) ~~on the surface, with the chip (CH) being mounted in a flip chip arrangement on the carrier substrate via by means of~~ electrically conductive connections between (BU), ~~and with the connecting areas (AF) being electrically connected to the electrically connective conductive structures and the connecting areas; and of the chip by means of electrically conductive connections (BU),~~
~~with a composite over the top surface of the chip, the composite comprising of a dielectric layer and a metal layer over it being positioned on the top side of the chip, with this composite being sealed to forming a seal with the carrier substrate outside of the an~~

area that corresponds to the chip; area, and with the chip

wherein the chip has a thickness being selected so such that the a force resulting
from forces arising due to thermal expansion of an electrically conductive connection the
aforementioned composite in the in a temperature range between -60° C and 85° C per one
electrically conductive connection or bump are is a maximum of 2 Newtons.

6. (Currently Amended) A component, containing comprising:

[[-]] a chip (CH) having a top surface and having a bottom surface that includes
electrically conductive structures; on the underside of the chip,

[[-]] a carrier substrate (TS), which has having a top surface that includes
connecting areas (AF) on the surface, with the chip (CH) being mounted in a flip chip
arrangement on the carrier substrate via by means of electrically conductive connections
between (BU), and with the connecting areas (AF) being electrically connected to the
electrically connective conductive structures and the connecting areas; and of the chip by
means of electrically conductive connections (BU),

[[-]] with a composite over the top surface of the chip, the composite comprising
of a dielectric layer and above it a metal layer positioned on above the dielectric layer
relative to the top side surface of the chip, with this the composite forming a seal with the
carrier substrate outside of an area that corresponds to the around the chip outside of the
chip; surface, and

[[-]] with wherein the dielectric layer having has a modulus of elasticity of less than
1 Gpa, a thickness of less than 20 µm, or a coefficient of thermal expansion which that is

greater than $\alpha_{bump}/2$ and that is less than $2 \alpha_{bump}$, where α_{bump} is the a coefficient of thermal expansion of for at least one of the electrically conductive connections (BU).

7. (Currently Amended) A component, containing comprising:

[-]] a chip (CH) having a top surface and having a bottom surface that includes
electrically conductive structures; on the underside of the chip;
[-]] a carrier substrate (TS), which has having a top surface that includes
connecting areas (AF) on the surface, with the chip (CH) being mounted in a flip chip
arrangement on the carrier substrate via by means of electrically conductive connections
between (BU), and with the connecting areas (AF) being electrically connected to the
electrically connective conductive structures and the connecting areas; and of the chip by
means of electrically conductive connections (BU);

[-]] a support element located on the top side surface of the carrier substrate, the
support element comprising in the form of a shrink frame, which that substantially
encircles the chip and tightly encloses the chip it.

8. (Currently Amended) The component as recited in of claim 7, wherein there is
further comprising a metal layer that substantially covers the top side surface of the chip;
and wherein the shrink frame and forms a seal with the carrier substrate.

9. (Currently Amended) The component as recited in one of claims claim 1, 5, 6,
or 7 through 8, wherein the chip has side surfaces that of the chip (CH) are sloped[,,] so

that ~~the~~ a cross-section of the chip tapers toward the carrier substrate (TS).

10. (Currently Amended) The component ~~as recited in one of claims~~ claim 1, 5, 6, or 7 through 9, wherein the chip has side surfaces ~~of the chip~~ (CH) have that comprise at least one step.

11. (Currently Amended) The component of claim 1 as recited in one of claims 1, 2, 9 or 10, wherein the seal covers ~~the~~ edge areas of the chip and ~~of~~ the support element; and surrounding it,

wherein with the seal does not cover the top side surface of the chip not being covered by the seal.

12. (Currently Amended) The component of claim 1 as recited in one of claims 1, 2 or 9 through 11, wherein there is further comprising a metal layer (ME) on the top side of the chip, on above the seal (AB) relative to the top surface of the chip, and the metal layer being on edge areas of the support element and/or ~~of~~ on edge areas of the carrier substrate that adjoin the seal and are not covered by it.

13. (Currently Amended) The component of claim 3 as recited in one of claims 3, 4, 9 or 10, wherein the dielectric layer (AB) completely covers the chip and (CH) together with the support element (SE) that encircles it, with this dielectric layer lying on the top side of the chip and on the support element, the dielectric layer and forming a seal with the

carrier substrate only ~~outside of~~ in areas that do not correspond to the support element[[],]
so that the chip and the support element ~~encircling~~ it are in a shared ~~cavity~~ which space
that is formed between the dielectric layer and the top side surface of the carrier substrate.

14. (Currently Amended) The component of claim 3 as recited in one of claims 3,
~~4, 9 or 10,~~ wherein the dielectric layer (AB) completely covers the top side surface of the
chip and seals it to the support element, ~~with the support element being of~~ comprising a
hermetically tight material.

15. (Currently Amended) The component of claim 3, further comprising as ~~recited~~
~~in one of claims 3 through 6, 9, 10, 13 or 14,~~ wherein there is a metal layer (ME) that
substantially covers ~~at least~~ the dielectric layer and ~~forms~~ composes with it.

16. (Currently Amended) The component of claim 3 as recited in one of claims 3
~~through 6, 9, 10 or 13 through 15,~~ wherein there is further comprising a filling compound
on the dielectric layer ~~or on the composite of the dielectric layer and the metal layer~~
~~outside of the chip.~~

17. (Currently Amended) The component as recited in of claim 16, wherein the
further comprising a metal layer that forms a seal with the support element outside of the
an area that corresponds to the chip area, or that forms a seal with the carrier substrate
outside of an area that corresponds to the support element.

18. (Currently Amended) The component of claim 1 or 7 as recited in claim 9 or 10, wherein there is further comprising a contact metallization (KM) on the side surfaces of the chip which that face toward the carrier substrate; (TS) or are sloping,

wherein the support element (SE) is in the form of comprises a solder frame on the top side of the carrier substrate, with the support element being soldered to the a contact metallization of the chip, and with the seal (AB) being formed by the solder frame.

19. (Currently Amended) The component as recited in of claim 18, wherein the top side of the chip is provided with further comprising a metal layer above a top surface of the chip.

20. (Currently Amended) The component of claim 1 as recited in at least one of claims 1, 2, 11 or 12, wherein the seal is made of comprises a dielectric material.

21. (Currently Amended) The component as recited in of claim 20, wherein the seal is made comprises at least one of a plastic, an organic plastic, a laminate film, a glass solder or and a resin.

22. (Currently Amended) The component of claim 3 as recited in one of claims 3, 4, 9, 10, 13 through 17, wherein the dielectric layer is made comprises at least one of a plastic, an organic plastic, a laminate film, a glass solder or and a resin.

23. (Currently Amended) The component of claim 1 as recited in at least one of claims 1 through 4, 9 through 17 or 20 through 22, wherein the support element ~~is made~~ comprises at least one of metal, a ceramic material or and plastic.

24. (Currently Amended) The component of claim 1 as recited in one of claims 1 through 4, 9 through 17 or 20 through 22, wherein the support element corresponds to a is the boundary of an indentation ~~provided~~ on the carrier substrate.

25. (Currently Amended) The component of claim 1 as recited in one of claims 1 through 4 or 9 through 24, wherein ~~the a~~ height of the support element does not exceed ~~the~~ a distance between the top side surface of the carrier substrate and ~~the a~~ bottom edge of the chip[[,]]; and

wherein an with the inner edge of the support element ~~reaching is~~ under the bottom edge of the chip that is ~~directed toward the carrier substrate~~.

26. (Currently Amended) The component of claim 1 as recited in at least one of claims 1 through 4, 9 through 17 or 20 through 24, wherein ~~the a~~ height of the support element ~~is equal to the~~ corresponds to, or exceeds, a distance between the top side surface of the carrier substrate and ~~the a~~ bottom edge of the chip ~~or exceeds~~ this distance.

27. (Currently Amended) The component of claim 1, 5, 6, or 7 as recited in one of

~~claims 1 through 26, wherein the carrier substrate (TS) is an LTCC ceramic [(-)]~~

comprises a low temperature cofired ceramic.

28. (Currently Amended) The component of claim 1, 5, 6, or 7 as recited in one of
~~claims 1 through 27, wherein there are further comprising surface-mounted-device-capable~~
[[SMD-capable]] external contacts (AK) ~~on the underside on a bottom surface~~ of the
carrier substrate (TS).

29. (Currently Amended) The component of claim 1, 5, 6, or 7 as recited in one
~~of claims 1 through 28, wherein the carrier substrate (TS) includes comprises~~ at least two
dielectric layers.

30. (Currently Amended) The component of claim 1, 5, 6, or 7 as recited in one of
~~claims 1 through 29, wherein the chip (CH) contains comprises~~ at least one resonator that
works with acoustic surface waves or acoustic volume waves.

31. (Currently Amended) The component of claim 1, 5, 6, or 7 as recited in one of
~~claims 1 through 30, which includes a plurality of like or differing further comprising~~
similar or different chips[[,] with the chips being that are attached on to the carrier
substrate and that are similarly encapsulated (TS) and encapsulated in the same manner.

32. (Currently Amended) A method for producing an encapsulated component

[[, -]] wherein using a chip having either (i) a chip with sloping side surfaces that taper
tapers toward the surface which bears electrically conductive structures, or (ii) a chip with
stepped side surfaces that have at least one step is used, with the side surfaces of the chip
having contact metallization, the method comprising:

[[-]] wherein there is applying metallization on the to a top side surface of a carrier
substrate; for placing a solder frame;

[[-]] wherein the applying a solder frame is produced on to the carrier substrate[[, -]];

[[-]] wherein placing the chip is placed on the carrier substrate and is soldered to it
in a flip chip arrangement; and construction;

[[-]] wherein the solder frame is soldered to the soldering contact metallization on
the side surfaces of the chip to the solder frame.

33. (Currently Amended) The method as recited in of claim 32, wherein prior to
soldering the chips to the solder frame, further comprising applying insulating non-
wettable structures IS are applied onto to the chip between the contact metallization of the
side surfaces and the electrically conductive structures associated with the chip.

34. (Currently Amended) The method as recited in of claim 32 or 33, wherein
further comprising applying a metal layer is applied to the a top side surface of the chip.

35. (Currently Amended) A method for producing an encapsulated component[[, -]]
using [[-]] wherein a chip is used which has having a surface with electrically conductive

structures, and using [[-]] wherein a substrate is used which has on its top side having a top surface with connecting areas for making contact with the chip and a frame that is capable of shrinking with a shrinkage behavior, the method comprising:

[[-]] wherein placing the chip is placed on the carrier substrate; is soldered soldering the chip to the carrier substrate it in a flip chip arrangement construction[[.]];

[[-]] wherein the frame is produced before the chip is placed on the carrier substrate, [[-]] wherein shrinking the frame is shrunk through temperature handling heating so that it the frame tightly encloses the chip[[.]]; and

[[-]] wherein forming a metal layer is produced which completely covers over the top side surface of the chip and the shrink frame.

36. (Currently Amended) The method as recited in of claim 35, [[-]] wherein one side of the frame is provided with comprises a connection layer, the connection layer comprising a solderable layer or with an adhesive layer[[.]]; and

[[-]] wherein connecting the frame is connected with to the carrier substrate by means of the aforementioned via the connection layer.

37. (Currently Amended) A method for producing an encapsulation for an electrical electric component, the method comprising with the following processing steps:

[[-]] attaching, to a carrier substrate, at least two chips carrying having conductive structures, the at least two chips being attached to the carrier substrate in a flip chip

arrangement via ~~are attached by means of~~ electrically conductive connections between connecting areas of the carrier substrate and (SU) in flip chip arrangement to a carrier substrate (TS), which has on its surface connecting areas (AF) for electrical connection with the electrically conductive structures of the chip[[,]];

[[-]] covering the at least two chips (CH) are covered with a dielectric layer (AB) which lies on the top side of the chip ~~that~~ and seals it together with to the carrier substrate[[,]] so that in this way each of the at least two chips is individually encapsulated and at least one space exists between the at least two chips[[,]]; and

[[-]] adding a filling compound to the at least one space between the at least two chips is filled with a filling compound (VM).

38. (Currently Amended) The method ~~as recited in~~ of claim 37, further comprising:

[[-]] wherein applying a metal layer (ME) that forms a composite with the dielectric layer (AB) is applied to the dielectric layer, the metal layer forming a composite with the dielectric layer; and

[[-]] wherein adding the filling compound (VM) is applied to the composite of the dielectric layer and the metal layer ~~outside of the chip~~.

39. (Currently Amended) The method ~~as recited in~~ of claim 37 or 38, wherein further comprising:

separating the carrier substrate ~~is then be sawed apart, so that to produce~~ individual

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components, wherein each of the individual components includes one of the at least two chips result which include at least one of the aforementioned chips.